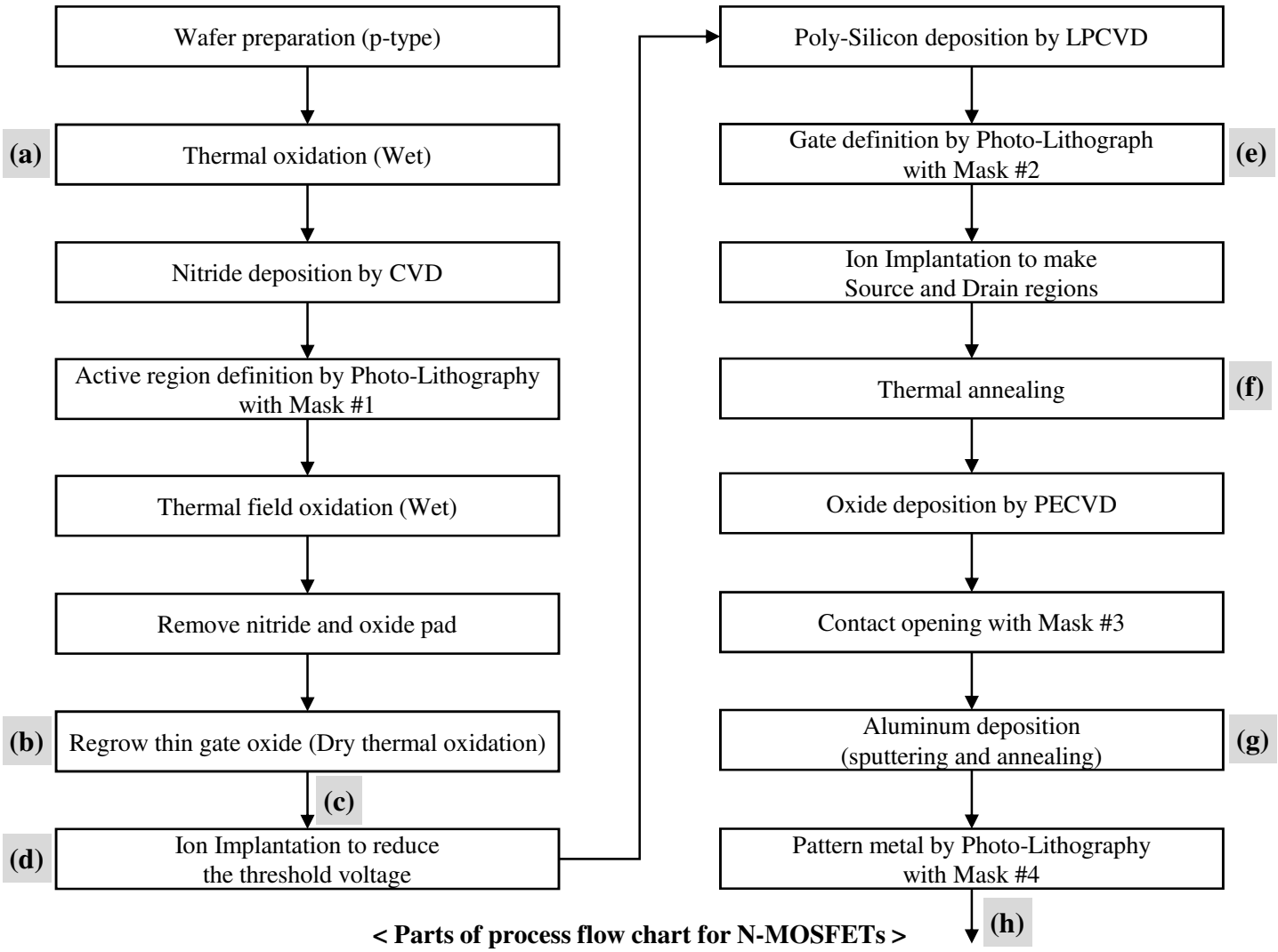
Final Exam (Total 50 points)

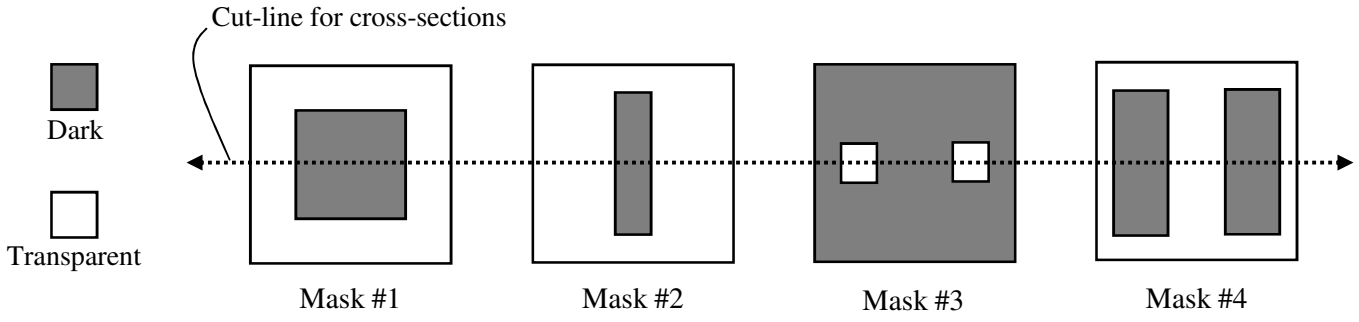
Professor: Sungsik Lee, **Subject:** Semiconductor Process (SP), Fall Semester in 2019
Graduate School, Department of Electronics Engineering, Pusan National University
Date: 19 Dec. 2019, **Duration:** 1 hour (14:00 ~ 15:00)

Solution

■ **Answer the questions on the next page while looking at the flow chart of the N-MOSFET process as seen below:**



< Parts of process flow chart for N-MOSFETs >

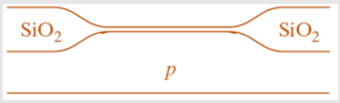


< Top view of masks for lithography with a positive PR >

Question 1 (6 points): Explain the process steps **(a) and (b)** in terms of a methodology itself, speed, and quality of the oxide.

(a) is done with H_2O, so higher speed growth but lower quality of oxide, suitable for FOx.
(b) is done directly with O_2, so lower speed growth but higher quality of oxide, suitable for gate Oxide.

Question 2 (6 points): Draw the cross-sectional view at the stage **(c).**



Question 3 (8 points): Explain the process details of **(d)** in terms of dopant types and implantation energy.

Threshold voltage reduction means to reduce the hole concentration of the p-type substrate,
so we should implant n-type dopants, such as P and As, to neutralize,
with a low energy implantation to form the doped region near the surface.

Question 4 (8 points): At the step **(e)**, we want to define the 10-nm-length as the minimum gate length.
Now, explain the requirements of optical source for the photo-lithography process.

L = 10nm is the minimum gate length, which means the feature size (F).
If the aperture (NA) is 1, F = 0.5 Lambda, at least.
So, optical source's wavelength should be at least smaller than 20nm.
This suggests EUV (13.5nm) as the optical source.

Question 5 (8 points): Provide reasons why we need the process step **(f)**, and what's the requirement of this.

After ion-implantation, the lattice gets damages.
So, we need a thermal annealing.
But, we should do this carefully, to minimize the impurity redistribution.
So, minimize D*t product, meaning a RTA (rapid thermal annealing).

Question 6 (8 points): At the step **(g)**, we need to choose the process temperature carefully. Now, explain why and how.

Aluminum and Silicon can be strongly alloyed at a high temperature as a commom melting point as the eutectic point.
The minimum eutectic point is around 577 degree Celsius.
At the temperature higher than 577, we get issues, such as Al-spike.
So, we should make Al-Si alloy at a temperature lower than 577.

Question 7 (6 points): Draw the cross-sectional view at the stage **(h).**